(Fed. Cir. 1986) (citing with approval, *Lindemann Maschinenfabrik v. American Hoist and Derrick*, 221 U.S.P.Q. 481, 485 (Fed. Cir. 1984)); *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

With respect to any of Claims 1, 2, 8, 9, 15 and 20, a determination of anticipation in accordance with Section 102 requires that each feature claimed therein be described in sufficient detail in *Webster* to enable one of ordinary skill in the art to make and practice the claimed invention.

In rejecting Claims 1, 8, and 20, the Examiner stated that:

> WEBSTER discloses for use in an integrated circuit of the type comprising at least two power supply domains (function circuits, column 4, line 7) in which each power supply domain comprises at least one module powered by the same voltage level, an apparatus for blocking an output signal in a first power supply domain from being sent to a second power supply domain when said second power supply domain is in a low power mode (column 5, lines 34-66, column 6, lines 1-50). (October 7, 2002 Office Action, Paragraph 2, Page 2).

The Applicant respectfully disagrees with the Examiner's assertions regarding the subject matter disclosed in the *Webster* reference. The Applicant respectfully submits that the *Webster* reference does not show each and every limitation of the Applicant's invention. The Applicant directs the Examiner's attention to Claim 1, which contains unique and novel limitations:

> 1. For use in an integrated circuit of the type comprising at least two power supply domains in which each power supply domain comprises at least one module powered by the same voltage level, an apparatus for blocking an output signal in a first power supply domain from being sent to a second power supply domain when said second power supply domain is in a low power mode. (Emphasis added).

The Applicant's invention is directed to an apparatus and method for blocking an output signal in a first power supply domain from being sent to a second power supply domain when the second power supply domain is in a low power mode. The Applicant's invention is also directed to an apparatus and method for blocking an output signal from a first power supply domain from being received in a second power supply domain when the first power supply domain is in a low power mode. The Applicant's invention prevents the occurrence of "Back Drive" problems. As described in the specification (Pages 13-14) "Back Drive" problems are created when a data signal that is correctly sent from an active power supply domain is incorrectly received by an inactive power supply domain.

Webster does not disclose, teach or suggest an apparatus and method for blocking an output signal in a first power supply domain from being sent to a second power supply domain when the second power supply domain is in a low power mode. *Webster* also does not disclose, teach or suggest an apparatus and method for blocking an output signal from a first power supply domain from being received in a second power supply domain when the first power supply domain is in a low power mode.

Webster discloses a power management apparatus for an integrated circuit in which "the power to a functional circuit contained in an integrated circuit is not completely removed, but decreased such that the functional circuit is placed in a reduced power mode of operation." (*Webster*, Column 2, Lines 50-53).

The Applicant respectfully traverses the assertion of the Examiner that the functional circuit 99 of *Webster* is equivalent to a power supply domain of the type described by the Applicant. *Webster's* definition of a functional circuit (*Webster*, Column 4, Lines 7-8) states that a functional circuit is "a means for performing a specified electronic function or group of electronic functions." Generally speaking, this definition of a functional circuit does not imply that the functional circuit comprises at least two power supply domains. There are many functional circuits that operate with only one power supply.

Webster shows a Power In Net No. 1 (40) of functional circuit 99 that may be considered analogous to a power supply domain. In the prior art circuit shown in Figure 1 of *Webster* Power In Net No. 1 (40) receives power from Power In Pad No. 1 (20). *Webster* also shows a plurality of "Power In Net" modules (up to Power In Net No. P (41)) within functional circuit 99. In the prior art circuit shown in Figure 1 of *Webster* Power In Net No. P (41) receives power from Power In Pad No. P (21).

In the apparatus of *Webster* shown in Figures 2 through 4 *Webster* places a "variable power source" (VPS) circuit between each "Power In Pad" (located at the edge of integrated circuit 201,

202 and 203) and its corresponding "Power In Net" (located in functional circuit 99). For example, Variable Power Source No. 1 (60) is located between Power In Pad No. 1 (20) and Power In Net No. 1 (40). Variable Power Source No. 1 (60) converts a first voltage level to a second voltage level and provides the second voltage level to Power In Net No. 1 (40) (*Webster*, Column 11, Lines 54-65).

Similarly, Variable Power Source No. P (61) is located between Power In Pad No. P (21) and Power In Net No. P (41). Variable Power Source No. P (61) converts a first voltage level to a second voltage level and provides the second voltage level to Power In Net No. P (41) (*Webster*, Column 11, Line 66 to Column 12, Line 10). *Webster* controls the plurality of Variable Power Sources with Power Control Pad 26.

Each Power In Net in functional circuit 99 is coupled to its own corresponding Power In Pad through its own corresponding Variable Power Source. That is, each Variable Power Source is exclusively coupled to its own Power In Net. For example, there is no connection between Variable Power Source No. 1 (60) and Power In Net No. P (41).

Furthermore, *Webster* does not disclose any communication between the various Power In Net modules in functional circuit 99. There is no mention of any communication between Power In Net No. 1 (40) and Power In Net No. P (41). Therefore, it is clear that *Webster* is completely silent concerning the concept of sending a signal from a first power supply domain to a second power supply domain. Accordingly, there is nothing in *Webster* that discloses, teaches or suggests the

concept of sending signals (or blocking signals) between two power supply domains. There is nothing in *Webster* than discloses, teaches or suggests the concept of sending signals (or blocking signals) between two power supply domains based upon the state of the power level of one of the two power supply domains.

The Applicant respectfully traverses the assertion of the Examiner that *Webster* comprises "an apparatus for blocking an output signal in a first power supply domain from being sent to a second power supply domain when said second power supply domain is in a low power mode (column 5, lines 34-66, column 6, lines 1-50)." Nothing in the portion of the *Webster* patent cited by the Examiner (or in any other portion of the *Webster* patent) recites the unique and novel claim limitations of Claim 1, Claim 8 and Claim 20 of the present patent application.

With respect to Claim 2 and Claim 9 the Examiner stated that *Webster* does not disclose a power sense cell. The Applicant agrees that *Webster* does not disclose a power sense cell. The Examiner then asserted that a Variable Power Source unit of *Webster* inherently comprises a power sense cell. (October 7, 2002 Office Action, Page 3, Lines 1-5). For the reasons set forth below, the Applicant respectfully traverses the assertion that a Variable Power Source unit of *Webster* inherently comprises a power sense cell.

The definition of the term "Variable Power Source" in *Webster* (Column 4, Line 37 to Column 5, Line 2) states that a variable power source comprises (1) a control input terminal, (2) a power input terminal, and (3) a power output terminal. "As used herein, when the control input

terminal is asserted, the variable power source converts a first voltage within a specified range of values present at its power input terminal to a second voltage within a specified range of values at its power output terminal." (*Webster*, Column 4, Lines 46-50). The control signal is provided to the variable power sources through Power Control Pad 26. "A voltage capable of asserting the control input terminals of Variable Power Source #1 60 through Variable Power Source #P 61, and I/O Switch # 1 62 through I/O Switch # K 63 is applied to Power Control Pad 26 by an external agent (not shown)." (Webster, Column 11, Lines 43-47) (Emphasis added).

There is no disclosure, teaching or suggestion in the portion of the *Webster* patent cited by the Examiner (or in any other portion of the *Webster* patent) that a power sense cell is inherent in the Variable Power Source units of *Webster*. The Variable Power Source units passively receive a control signal from an external source. The Variable Power Source units do not actively sense the power levels of portions of functional circuit 99. Therefore, the Variable Power Source units of *Webster* do not inherently comprise power sense cells. *Webster* does not anticipate the subject matter of Claim 2 and of Claim 9 of the present patent application.

For the reasons set forth above, the Applicant also respectfully traverses the Examiner's rejection of Claim 15. *Webster* does not use a power sense cell to detect when a power supply domain is in a low power mode. *Webster* does not block an output signal from a first power supply domain from being sent to a second power supply domain. *Webster* does not anticipate the subject matter of Claim 15 of the present patent application.

Claim Rejections 35 U.S.C. § 103

In Paragraphs 3-4 on Pages 4-6 of the October 7, 2002 Office Action the Examiner rejected Claims 3, 4, 10, 11, 16, 17, 21 and 22 under 35 U.S.C. § 103(a) as being unpatentable over *Webster*. The Examiner also rejected Claims 5, 6, 7, 12, 13, 14, 18, 19, 23 and 24 under 35 U.S.C. § 103(a) as being unpatentable over *Webster* in view of United States Patent No. 5,848,281 issued to *Smalley et al.* (hereafter "*Smalley*").

The Applicant respectfully traverses the rejection of Claims 3-7, 10-14, 16-19 and 21-24. The Applicant respectfully requests the Examiner to withdraw the rejections of the above referenced claims in view of the Applicant's remarks concerning the prior art references.

During *ex parte* examinations of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of non-obviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does

not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 USPQ 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not be based on an applicant's disclosure. MPEP § 2142.

The Applicant respectfully submits that the Patent Office has not established a *prima facie* case of obviousness with respect to the Applicant's invention. The Applicant reiterates the arguments that the Applicant has previously made with respect to the *Webster* reference. There is no teaching, suggestion or even a hint in the *Webster* reference concerning the Applicant's novel and unique concepts of (1) blocking an output signal in a first power supply domain from being sent to a second power supply domain when the second power supply domain is in a low power mode, and

(2) blocking an output signal from a first power supply domain from being received in a second power supply domain when the first power supply domain is in a low power mode. A teaching or suggestion to make the Applicant's invention and a reasonable expectation of success is not found in the *Webster* reference (or in any other prior art reference). Therefore, the Applicant's invention is not *prima facie* obvious in view of the *Webster* reference.

With respect to Claims 3, 4, 10, 11, 16, 17, 21 and 22 the Examiner has stated that "WEBSTER discloses functional circuits and a logical term, deasserted state, implying that a logical function has taken place (column 4, line 21)." (October 7, 2002 Office Action, Paragraph 4, Page 4). The Applicant agrees that *Webster* discloses a functional circuit. The Applicant respectfully disagrees that the *Webster* definition of the term "deasserted state" as a "logical term" in Column 4, Line 21 implies that the *Webster* apparatus is capable of performing a "logical function" of the type disclosed and claimed by the Applicant. There must be some actual circuit disclosed in *Webster* that can perform the allegedly implied "logical function."

As previously mentioned, the control signal to each of the Variable Power Sources in *Webster* is provided by Power Control Pad 26. The control signal is provided by an external agent (not shown)." (*Webster*, Column 11, Lines 43-47) (Emphasis added). There is no showing that *Webster* uses logic circuits to "receive logic levels from a power sense cell." This is because *Webster* does not have any power sense cells. There is no showing that *Webster* uses logic levels from a power sense cell to send or block signals between power supply domains. In short, *Webster*

is completely silent on the subject matter of Claims 3, 4, 10, 11, 16, 17, 21 and 22. The Applicant respectfully traverses the Examiner's assertion that Claims 3, 4, 10, 11, 16, 17, 21 and 22 are obvious in view of *Webster*.

With respect to Claims 5, 6, 12, 13, 18, 19, 23 and 24 the Examiner has stated that "WEBSTER discloses the apparatus as claimed in claim 2." For the reasons set forth above, the Applicant respectfully traverses the Examiner's assertion that *Webster* discloses the Applicant's invention as claimed in Claim 2. The Examiner also stated that "WEBSTER does not disclose a schmitt trigger." The Applicant agrees that *Webster* does not disclose a Schmitt trigger.

The Examiner also stated that "SMALLEY discloses a schmitt trigger (column 7, lines 42-49) device operated as a synchronizer circuit for synchronizing the asynchronous sleep and idle signals with the clock signal. It would have been obvious to one having ordinary skill in the art at the time of this invention to provide an apparatus as claimed in claim 2 wherein said power sense cell comprises a schmitt trigger circuit and an apparatus for synchronizing blocked clock signals to prevent clock signals from being shortened by a signal from said power sense cell in order to maintain sensing transition to only occur during a clock transition to maintain system synchronization." (October 7, 2002 Office Action, Page 5). The Applicant respectfully traverses the Examiner's assertion that it would have been obvious to combine the *Webster* reference with the *Smalley* reference.

Under the applicable patent law, there must be some teaching, suggestion or motivation to combine the *Webster* reference and the *Smalley* reference. "When a rejection depends on a combination of prior art references, there must be some teaching, or motivation to combine the references." *In re Rouffet*, 149 F.3d 1350, 1355-56, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998). "It is insufficient to establish obviousness that the separate elements of an invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the references." *Arkie Lures, Inc. v. Gene Larew Tackle, Inc.*, 119 F.3d 953, 957, 43 USPQ2d 1294, 1297 (Fed. Cir. 1997). The Applicant respectfully submits that there exists no teaching, suggestion or motivation in the prior art to combine the teachings of the *Webster* reference and the teachings of the *Smalley* reference.

When two references are combined the combination of the references must teach or suggest all the claim limitations. In the present case, even if the *Webster* reference were combined with the *Smalley* reference, the combination of the *Webster* reference and the *Smalley* reference would not teach, suggest or even hint at the Applicant's invention. This is because neither the *Webster* reference nor the *Smalley* reference teaches, suggests, or even hints at the Applicant's concepts of (1) using power sense cells to detect power levels of separate power supply domains, or (2) blocking an output signal in a first power supply domain from being sent to a second power supply domain when the second power supply domain is in a low power mode, or (3) blocking an output signal from a first power supply domain from being received in a second power supply domain when the

first power supply domain is in a low power mode. The Applicant respectfully submits that th rejections of Claims 5, 6, 12, 13, 18, 19, 23 and 24 under 35 U.S.C. §103(a) combining the *Webster* reference and the *Smalley* reference should be withdrawn.

With respect to Claim 7 and Claim 14 the Examiner has stated that "It would have been obvious to one having ordinary skill in the art at the time of this invention to merely arrange D flip flops and logic gates to generate control signals to control a power management apparatus for integrated circuit applications." (October 7, 2002 Office Action, Page 6). For the reasons set forth above, the Applicant respectfully traverses the Examiner's assertion that it would be obvious to combine the teachings of *Webster* with the teachings of *Smalley*.

When two references are combined the combination of the references must teach or suggest all the claim limitations. In the present case, even if the *Webster* reference were combined with the *Smalley* reference, the combination of the *Webster* reference and the *Smalley* reference would not teach, suggest or even hint at the Applicant's invention in Claim 7 or in Claim 14. This is because neither the *Webster* reference nor the *Smalley* reference teaches, suggests, or even hints at the Applicant's concepts of (1) using power sense cells to detect power levels of separate power supply domains, or (2) blocking an output signal in a first power supply domain from being sent to a second power supply domain when the second power supply domain is in a low power mode, or (3) blocking an output signal from a first power supply domain from being received in a second power supply domain when the first power supply domain is in a low power mode. The Applicant

respectfully submits that the rejections of Claim 7 and Claim 14 under 35 U.S.C. §103(a) combining the *Webster* reference and the *Smalley* reference should be withdrawn.

The Applicant respectfully submits that Claims 1-24 are all patentable over the *Webster* reference and the *Smalley* reference whether taken individually or in combination. The Applicant respectfully requests that the rejection of Claims 1-24 be withdrawn and that Claims 1-24 be passed to issue.

The Applicant's attorney has made the amendments herein and the arguments set forth above in order to place this Application in condition for allowance. In the alternative, the Applicant's attorney is making the same to properly frame the issues for appeal. In this Amendment, the Applicant makes no admission concerning any now moot rejection or objection, and affirmatively denies any position, statement or averment of the Examiner that was not specifically addressed herein.

SUMMARY

The Applicant respectfully requests consideration and allowance of the above claims. If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com.*

The Commissioner is hereby authorized to charge any additional fees connected with this Amendment or credit any overpayment to National Semiconductor Deposit Account No. 14-0448.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: Jan. 30, 2003

William A. Munck
Registration No. 39,308

P. O. Drawer 800889
Dallas, Texas 75380
Tel: (972) 628-3600
Fax: (972) 628-3616
Email: wmunck@davismunck.com